This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) An LDMOS transistor array structure comprising:

an array that includes a plurality of alternating source regions and a plurality of alternating drain regions formed in a semiconductor substrate to define a checkerboard pattern of said alternating source and drain regions, wherein at least a first source region of the alternating source regions includes a first source region outer face which is orientated toward a first drain region face of a first drain region of the plurality of alternating drain regions, and wherein the first drain region face has a drain region face length and the source region outer face has a source region face length, and wherein the drain region face length is greater than the source region face length, wherein the first source region is disposed between the first drain region and a second drain region, and the first source is the only source region between the first drain region and the second drain region and the first source region is a contiguous region having a first conductivity type;

a conductive source region interconnect structure formed in electrical contact with each of the plurality of alternating source regions in the array to electrically connect said source regions in parallel; and

a conductive drain region interconnect structure formed in electrical contact with each of the plurality of alternating drain regions in the array to electrically connect said drain regions in parallel.

2. (Original) The LDMOS transistor array structure as in claim 1, wherein the drain region face length is at least 1.5 times greater than the source region face length.

3. (Original) The LDMOS transistor array structure as in claim 1, wherein the drain region face length is at least twice as long as the source region face length.

4. (Currently Amended) The LDMOS transistor array structure as in claim 1, wherein the source region outer face has a source region face depth, and the drain region face has a drain region face depth, and the source region face depth and the drain region face depth are substantially equal in length.

5. (Currently Amended) An LDMOS transistor array structure as in claim 1, wherein each of the alternating source regions has four source region outer faces, and each of the source region outer faces has the same source region face length, and wherein each of the alternating drain regions has four faces, and each of the drain region faces has the same drain region face length.

6. (Original) The LDMOS transistor array structure as in claim 5, wherein the drain region face length is at least 1.5 times greater than the source region face length.

7. (Original) The LDMOS transistor array structure as in claim 5, wherein the drain region face length is at least twice as long as the source region face length.

8. (Currently Amended) The LDMOS transistor array structure as in claim 5, wherein the source region outer faces have a source region face depth, and the drain region faces have a drain region face depth, and the source region face depth and the drain region face depth are substantially equal in length.

9. (Previously Presented) An high power transistor, including:

a source region which includes a first source region outer face wherein the source region outer face has a source region face length, wherein the source region is a contiguous region of first conductivity type;

a first drain region which includes a first drain region face wherein the first drain region face has a drain region face length;

a second drain region which includes a second drain region face wherein the second drain region face has the drain region face length;

wherein the source region is the only source region disposed between the first drain region face and the second drain region face;

a source contact coupled with the source region;

a drain contact coupled with the first drain region, and the second drain region;

a channel region disposed between the source region and the first drain region face and a second channel between the source region and the second drain region face;

wherein in response to a voltage applied across the source contact and the drain contact electrons flow from the source region to the first drain region and the second drain region; and

wherein the drain region face length is longer than the source region face length.

10. (Original) The high power transistor as in claim 9, wherein the drain region face length is at least 1.5 times greater than the source region face length.

11. (Original) The high power transistor as in claim 9, wherein the drain region face length is at least twice as long as the source region face length.

12. (Currently Amended) The high power transistor as in claim 9, wherein the source region outer face has a source region face depth, and the drain region face has a drain region face depth, and the source region face depth and the drain region face depth are substantially equal in length.

13. (Original) The high power transistor as in claim 9, further including:

a plurality of alternating source regions each source region including four source region faces, and each of the source region faces has the same source region face length;

a plurality of alternating drain regions, each of the drain regions having four faces, and each of the drain region faces has the same drain region face length.

14. (New) An LDMOS transistor array structure comprising:

an array that includes a plurality of alternating source regions and a plurality of alternating drain regions formed in a semiconductor substrate to define a checkerboard

pattern of said alternating source and drain regions, wherein at least a first source region of the alternating source regions includes a first source region face which is orientated toward a first drain region face of a first drain region of the plurality of alternating drain regions, and wherein the first drain region face has a drain region face length and the source region face has a source region face length, and wherein the drain region face length is greater than the source region face length, wherein the first source region is disposed between the first drain region and a second drain region, and the first source is the only source region between the first drain region and the second drain region and the first source region is a contiguous region having a first conductivity type;

a conductive source region interconnect structure formed in electrical contact with each of the plurality of alternating source regions in the array to electrically connect said source regions in parallel;

a conductive drain region interconnect structure formed in electrical contact with each of the plurality of alternating drain regions in the array to electrically connect said drain regions in parallel; and

wherein the drain region face length is at least twice as long as the source region face length.

15. (New) An LDMOS transistor array structure as in claim 14, wherein each of the alternating source regions has four source region faces, and each of the source region faces has the same source region face length, and wherein each of the alternating drain regions has four faces, and each of the drain region faces has the same drain region face length.

16. (New) An high power transistor, including:

a source region which includes a first source region face wherein the source region face has a source region face length, wherein the source region is a contiguous region of first conductivity type;

a first drain region which includes a first drain region face wherein the first drain region face has a drain region face length;

a second drain region which includes a second drain region face wherein the second drain region face has the drain region face length;

wherein the source region is the only source region disposed between the first drain region face and the second drain region face;

a source contact coupled with the source region;

a drain contact coupled with the first drain region, and the second drain region;

a channel region disposed between the source region and the first drain region face and a second channel between the source region and the second drain region face;

wherein in response to a voltage applied across the source contact and the drain contact electrons flow from the source region to the first drain region and the second drain region;

wherein the drain region face length is longer than the source region face length; and

wherein the drain region face length is at least twice as long as the source region face length.